22. (Amended) The semiconductor memory according to claim 21, wherein said voltage generator circuit includes:

a first circuit supplied with [an] the operating voltage so as to provide [a] the first voltage to said plurality of word driver circuits;

a second circuit supplied with the operating voltage so as to provide the first voltage to said plurality of word driver circuits;

wherein said first circuit provides the first voltage in response to the first signal from the outside of the chip; and

wherein said second circuit provides said small output current to said plurality of word driver circuits in order to keep the output voltage of said voltage generator circuit to the first voltage while said first circuit stops providing the first voltage to said plurality of word driver circuits.

Please cancel claims 29 - 33 without prejudice.

Please add the following new claims:

34. A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of memory cells, for storing data, each cell having at least a transfer MOS transistor;

a plurality of word lines, each word line coupled with gate electrodes of a subset of said transfer MOS transistors of said plurality of memory cells;

a plurality of word driver circuits [for] each providing an output voltage to a word line of said plurality of word lines;

a voltage generator circuit supplied with an operating voltage so as to provide a first voltage to said word driver circuit;

wherein the amplitude of said first voltage is larger than that of said operating voltage so that said plurality of word driver circuits can provide the output voltage [whose] at an amplitude [is] larger than an amplitude of an input voltage;

wherein said voltage generator circuit provides a small output current to said plurality of word driver circuits in order to keep the output voltages thereof to the first voltage when none of said plurality of word lines is selected, and provides a large output current to said one of plurality of word driver circuits in response to a first signal from an outside of the chip;

wherein each of said plurality of word driver circuits brings its associated word line to a predetermined potential lower than said first voltage when said associated word line is not selected; and

wherein each of said plurality of word driver circuits establishes a current path between the first voltage and its associated word line, raising the potential on said associated word line to the first voltage, when said associated word line is selected.

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, ~~and~~ a first power receiving node, and a P-channel MOS transistor having a source-drain path which is coupled between the first power receiving node and the first output node;

a voltage generator circuit having a second output node coupled to the first power receiving nodes of said plurality of word drivers, and a second power receiving node to which an operating voltage is supplied;

wherein said voltage generator circuit produces a first voltage which is larger than the operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected,

wherein each of said plurality of word drivers brings its corresponding word line to a first predetermined potential, lower than said first voltage, when said corresponding word line is not selected; and

wherein the P-channel MOS transistor of a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage.

35. The semiconductor memory according to claim 34,

wherein said voltage generator circuit has a first operation mode and a second operation mode;

wherein the amount of current supplied when in said first operation mode is larger than that of said operation second mode; and

wherein said voltage generator circuit is in said first operation mode when one of said word lines is selected.

36. The semiconductor memory according to claim 35,

wherein said voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the second output node, and a detector circuit whose input is coupled to the second output node,

wherein the detector circuit outputs a control signal when the first voltage is larger than a second predetermined potential, and

wherein a voltage level of the first voltage is kept to the second predetermined potential through intermittent operation of the charge pump circuit in response to the control signal.

37. The semiconductor memory according to claim 34,

wherein said voltage generator circuit also includes a voltage clamp circuit, clamping the first voltage to a second predetermined potential, coupled to the output node.

38. The semiconductor memory according to claim 34,

wherein the first voltage is supplied to gates of the P-channel MOS transistors of each of said plurality of word drivers when its corresponding word line is not selected.

39. The semiconductor memory according to claim 38,

wherein said voltage generator circuit has a first operation mode and a second operation mode, and

wherein the amount of current supplied by said voltage generator circuit when in said first operation mode is larger than that supplied when in said second operation mode, and

wherein said voltage generator circuit is in said first operation mode when one of said word lines is selected.

40. The semiconductor memory according to claim 39,

wherein said voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the second output node, and a detector circuit whose input is coupled to the second output node,

wherein the detector circuit outputs a control signal when the first voltage is larger than a second predetermined potential, and

wherein a voltage level of the first voltage is kept to the second predetermined potential through intermittent operation of the charge pump circuit in response to the control signal.

41. The semiconductor memory according to claim 34, wherein the operating voltage is a external voltage which is supplied form an outside of the chip.

42. A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, and a first power receiving node;

a voltage generator circuit having a second output node coupled to the first power receiving nodes of said plurality of word drivers, and a second power receiving node to which an operating voltage is supplied;

wherein said voltage generator circuit produces a first voltage which is larger than the operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected;

wherein each of said plurality of word drivers brings its corresponding word line to a predetermined potential, lower than said first voltage, when said corresponding word line is not selected;

wherein a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage; and

wherein the amount of current supplied when in said first mode is larger than that of said second mode.

16 ~~43~~. The semiconductor memory according to claim 15 ~~42~~,

wherein each one of said plurality of word drivers also includes a P-channel MOS transistor having a source-drain path which is coupled between the first power receiving node and the first output node;

wherein the P-channel MOS transistor of a selected one of said plurality of word drivers is turned ON when the corresponding one of said plurality of word lines is selected; and

wherein the first voltage is supplied to gates of the P-channel MOS transistors of each of said plurality of word drivers when its corresponding word line is not selected.

17 ~~44~~. The semiconductor memory according to claim 15 ~~42~~,

wherein said voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the second output node, and a detector circuit whose input is coupled to the second output node,

wherein the detector circuit outputs a control signal when the first voltage is larger than a second predetermined potential, and

wherein a voltage level of the first voltage is kept to the second predetermined potential by through intermittent operation of the charge pump circuit in response to the control signal.

18 ~~48~~. The semiconductor memory according to claim 17 ~~44~~,

wherein said voltage generator circuit also includes another charge pump circuit whose output is coupled to the second output node, and

wherein the other charge pump circuit produces the first voltage when one of said plurality of word lines is selected.

19 ~~46~~. The semiconductor memory according to claim 18 ~~45~~,

wherein the other charge pump circuit produces the first voltage in response to a signal which indicates a start of accessing said plurality of memory cells.

20 ~~47~~. The semiconductor memory according to claim 19 ~~46~~, wherein the signal is a row address strobe signal.

21 ~~48~~. The semiconductor memory according to claim 15 ~~42~~,

wherein said voltage generator circuit also includes a voltage clamp circuit, clamping the first voltage to a predetermined potential, coupled to the second output node.

22 ~~49~~. The semiconductor memory according to claim 15 ~~42~~, wherein the operating voltage is an external voltage which is supplied from outside of the chip.

50. A semiconductor memory in a chip, comprising:

plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a first subset of said plurality of dynamic memory cells;

a plurality of data lines, each data line coupled to the source or drain electrode of one of said transfer MOS transistors of a second subset of said plurality of memory cells;

a plurality of sense amplifiers, each sense amplifiers having a input/output node coupled to a corresponding one of said plurality of data lines;

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, and a first power receiving node;

a voltage generator circuit having a second output node coupled to the first power receiving node of each of said plurality of word drivers;

a voltage limiter circuit having a third power receiving node to which an external voltage is supplied, and a third output node providing an internal voltage;

wherein said voltage generator circuit produces a first voltage which is larger than the operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected;

wherein each of said plurality of word drivers brings its corresponding word line to a predetermined potential, lower than said first voltage, when said corresponding word line is not selected;

wherein a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage;

wherein a signal of the corresponding one of said plurality of data lines read from the corresponding one of said plurality of memory cells is amplified to a first potential or second potential by the corresponding one of said plurality of sense amplifiers;

wherein the first potential is larger than the second potential;

wherein the first potential is clamped to a voltage level of the internal voltage, wherein the internal voltage is smaller than the external voltages, and

wherein a level of the first voltage is larger than the first potential.

51. The semiconductor memory according to claim 50, wherein said voltage generator circuit has a first operation mode and a second operation mode, the amount of current being supplied by said voltage generator for circuit in said first operation mode being more than the amount of current supplied in said second operation mode, and

wherein said voltage generator circuit is in the first operation mode when one of said plurality of word lines is selected.

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~~52~~. The semiconductor memory according to claim ~~50~~, wherein said voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the second output node, and a detector circuit whose input is coupled to the second output node;

wherein the detector circuit outputs a control signal when the first voltage is larger than a second predetermined potential; and

wherein a voltage level of the first voltage is kept to the second predetermined potential by through intermittent operation of the charge pump circuit in response to the control signal.

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~~53~~. The semiconductor memory according to claim ~~50~~, wherein each one of said plurality of word drivers also includes a P-channel MOS transistor having a source-drain path which is coupled between the first power receiving node and the first output node;

wherein the P-channel MOS transistor of a selected one of said plurality of word drivers is turned ON when the corresponding one of said plurality of word lines is selected; and

wherein the first voltage is supplied to gates of the P-channel MOS transistors of each of said plurality of word drivers when its corresponding word line is not selected.

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~~54~~. The semiconductor memory according to claim ~~50~~, wherein said voltage generator circuit also includes a voltage clamp circuit, clamping the first voltage to a second predetermined potential, coupled to the second output node.

29 ~~55~~. The semiconductor memory according to claim 23 ~~50~~, wherein a voltage change of the internal voltage is less than a voltage change of the external voltage.

29 ~~56~~. The semiconductor memory according to claim 24 ~~51~~, wherein a voltage change of the internal voltage is less than a voltage change of the external voltage.

30 ~~57~~. The semiconductor memory according to claim 25 ~~52~~, wherein a voltage change of the internal voltage is less than a voltage change of the external voltage.

31 ~~58~~. The semiconductor memory according to claim 26 ~~53~~, wherein a voltage change of the internal voltage is less than a voltage change of the external voltage.

32 ~~59~~. The semiconductor memory according to claim 23 ~~50~~, wherein the first voltage is larger than the external voltage.

33 ~~60~~. The semiconductor memory according to claim 24 ~~51~~, wherein the first voltage is larger than the external voltage.

34 ~~61~~. The semiconductor memory according to claim 25 ~~52~~, wherein the first voltage is larger than the external voltage.

35 ~~62~~. The semiconductor memory according to claim 26 ~~53~~ ~~52~~, wherein the first voltage is larger than the external voltage.

36 ~~63~~. A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

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a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, and a first power receiving node;

a voltage generator circuit having a second output node coupled to the first power receiving nodes of said plurality of word drivers, a first and a second charge pump circuit each having an output coupled to the second output node, and a second power receiving node, coupled to the first and the second charge pump circuit, to which an operating voltage is supplied;

wherein said voltage generator circuit produces a first voltage which is larger than the operating voltage in both a first and a second operation mode;

wherein each of said plurality of word drivers brings its corresponding word line to a predetermined potential, lower than said first voltage, when said corresponding word line is not selected;

wherein a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage;

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wherein the first charge pump circuit is operative in the first operation mode when one of said plurality of word lines is selected;

wherein the second charge pump circuit is operative in the second operation mode when none of said plurality of word lines is selected; and

wherein a current supplying capability of the first charge pump circuit is larger than that of the second charge pump circuit.

37. The semiconductor memory according to claim 36, wherein each one of said plurality of word drivers also includes a P-channel MOS transistor having a source-drain path which is coupled between the first power receiving node and the first output node;

wherein the P-channel MOS transistor of a selected one of said plurality of word drivers is turned ON when the corresponding one of said plurality of word lines is selected, and

wherein the first voltage is supplied to gates of the P-channel MOS transistors of each of said plurality of word drivers when its corresponding word line is not selected.

38. The semiconductor memory according to claim 36, wherein said voltage generator circuit also includes a voltage clamp circuit, clamping the first voltage to a second predetermined potential, coupled to the second output node.

66. The semiconductor memory according to claim 63, wherein the first charge pump circuit produces the first voltage in response to a signal which indicates a start of accessing said plurality of memory cells.

67. The semiconductor memory according to claim 66, wherein the signal is a row address strobe signal.

68. A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of word drivers, each word driver having:

a first output node coupled to a corresponding one of said plurality of word lines;

a first power receiving node;

a P-channel MOS transistor having;

a source-drain path which is coupled between the first power receiving node and the first output node; and

a gate electrode coupled to a selection node to which a signal selecting its corresponding word line may be supplied to close said source-drain path;

said first output supplying a predetermined potential, lower than a first voltage, when said corresponding word line is not selected; and

a voltage generator circuit having:

a second output node coupled to the first power receiving nodes of each of said plurality of word drivers:

having a second power receiving node to receive an operating voltage; and

producing, at said second output node, the first voltage which is larger than the supplied operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected.

42. The semiconductor memory according to claim 41,

wherein the voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the second output node, and a detector circuit having an input coupled to the second output node, and having an output which outputs a control signal when the first voltage is larger than a second predetermined potential, said charge pump circuit being operative in response to said control signal.

43. The semiconductor memory according to claim 41,

wherein each word driver includes a circuit coupling the first voltage to the gate of its P-channel MOS transistor when the selecting signal is not supplied to the selection node.

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71. The semiconductor memory according to claim 68,

wherein the voltage generator circuit includes a first circuit and a second circuit, the current supply capability of the first circuit being greater than that of the second circuit, the first circuit being operative in response to selection of one of said plurality of word lines.

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72. A method of operating a semiconductor memory in a chip, the semiconductor memory including a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor; a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells, and a gate driver for each individually selectable word line, having an output coupled to its associated word line, comprising:

supplying an operating voltage to the semiconductor memory;

producing, from the operating voltage, a first voltage which is larger than the operating voltage both in a first mode when one of said plurality of word lines is selected and in a second mode when none of said plurality of word lines is selected;

supplying said first voltage to each of said word drivers at a first current level when in the second mode;

coupling to each word line which is not selected, from its associated word driver output, a predetermined potential, lower than said first voltage;

entering said first mode and selecting a word line for reading; and

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in response to entry of said first mode, coupling said first voltage supplied to said word driver to its output, to raise the potential of the selected word line to said

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first voltage and increasing the current of said first voltage to a second predetermined level.

73. A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a voltage generator circuit:

having a first output node and a first power receiving node to receive an operating voltage; and

producing, at said first output node, a first voltage which is larger than the supplied operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected;

a plurality of word drivers, each word driver having:

a second output node coupled to a corresponding one of said plurality of word lines; and

a second power receiving node coupled to the first output node;

a P-channel MOS transistor having:

a source-drain path which is coupled between the second power receiving node and the second output node; and

a gate electrode coupled to a selection node to which a signal selecting its corresponding word line may be supplied to close said source-drain path of the P-channel MOS transistor; and

a N-channel MOS transistor having:

a source-drain path which is coupled between the second output node and a predetermined potential which is lower than the first voltage; and

a gate electrode coupled to the selection node to which the signal selecting its corresponding word line may be supplied to open said course-drain path of the N-channel MOS transistor.

47. The semiconductor memory according to claim 46, wherein the voltage generator circuit includes a charge pump circuit whose output produces the first voltage and is coupled to the first output node, and a detector circuit having an input coupled to the first output node, and having an output which outputs a control signal when the first voltage is larger than another predetermined potential, said charge pump circuit being operative in response to said control signal.

48. The semiconductor memory according to claim 46, wherein each word driver includes a circuit coupling the first voltage to the gate of its P-channel MOS transistor and the gate of its N-channel MOS transistor when the selection signal is not supplied to the selection node.